AMENDMENTS TO THE CLAIMS

Please add Claim 19, as indicated below.

Please amend Claims 1, 6, 8, and 12, as indicated below.

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough or in double brackets (e.g., ~~deletion~~ or [[deletion]]):

1. (Currently Amended) A memory module comprising:

a printed circuit board having a first lateral portion and a second lateral portion;

a plurality of identical integrated circuits mounted in at least two rows onto at least one surface of the printed circuit board;

a control logic bus connected to the plurality of identical integrated circuits; and

a first register and a second register connected to the control logic bus, the first register addressing the identical integrated circuits located ~~in a first row and a second row of identical integrated circuits~~ on [[a]]the first lateral portion ~~of the at least one surface of the printed circuit board~~ and not addressing the identical integrated circuits located on the second lateral portion, and the second register addressing the identical integrated circuits located ~~in the first row and the second row of identical integrated circuits~~ on [[a]]the second lateral portion ~~of the at least one surface of the printed circuit board~~ and not addressing the identical integrated circuits located on the first lateral portion.

2. (Original) The memory module of Claim 1, wherein the plurality of identical integrated circuits comprises Double Data Rate SDRAM.

3. (Original) The memory module of Claim 1, wherein the printed circuit board has approximate dimensions of 5.25 inches wide by 2.05 inches high.

4. (Original) The memory module of Claim 1, wherein the plurality of identical integrated circuits comprises 36 integrated circuits of type 256-Megabit SDRAM organized as 64 Meg by 4 bits.

5. (Original) The memory module of Claim 1, where in the plurality of identical integrated circuits comprises 36 integrated circuits of type 512-Megabit SDRAM organized as 128 Meg by 4 bits.

6. (Currently Amended) The memory module of Claim 1, wherein the identical integrated circuits located in [[the]]a first row of the first lateral portion ~~of the at least one surface~~

~~of the printed circuit board~~ have a first orientation direction and the identical integrated circuits located in [[the]]a second row of the first lateral portion ~~of the at least one surface of the printed circuit board~~ have a second orientation direction rotated in a plane parallel to the printed circuit board by an orientation angle.

7. (Previously Presented) The memory module of Claim 6, wherein the orientation angle is approximately 180 degrees.

8. (Currently Amended) The memory module of Claim 1, wherein the identical integrated circuits located in [[the]]a first row of the second lateral portion ~~of the at least one surface of the printed circuit board~~ have a first orientation direction and the identical integrated circuits located in [[the]]a second row of the second lateral portion ~~of the at least one surface of the printed circuit board~~ have a second orientation direction rotated in a plane parallel to the printed circuit board by an orientation angle.

9. (Original) The memory module of Claim 8, wherein the orientation angle is approximately 180 degrees.

10. (Previously Presented) The memory module of Claim 1, wherein the first lateral portion comprises a first lateral half of the printed circuit board.

11. (Previously Presented) The memory module of Claim 1, wherein the second lateral portion comprises a second lateral half of the printed circuit board.

12. (Currently Amended) A memory module comprising:

a printed circuit board;

a plurality of identical integrated circuits mounted in a first row and a second row onto at least one surface of the printed circuit board;

a control logic bus connected to the plurality of identical integrated circuits; and

a first register and a second register connected to the control logic bus, the first register addressing only the identical integrated circuits located in the first row and the second row of identical integrated circuits on a first lateral portion of the at least one surface of the printed circuit board, and the second register addressing only the identical integrated circuits located in the first row and the second row of identical integrated circuits on a second lateral portion of the at least one surface of the printed circuit board.

13. (Previously Presented) The memory module of Claim 12, wherein the first lateral portion comprises a first lateral half of the printed circuit board.

14. (Previously Presented) The memory module of Claim 12, wherein the second lateral portion comprises a second lateral half of the printed circuit board.

15. (Previously Presented) The memory module of Claim 12, wherein the identical integrated circuits located in the first row of the first lateral portion of the at least one surface of the printed circuit board have a first orientation direction and the identical integrated circuits located in the second row of the first lateral portion of the at least one surface of the printed circuit board have a second orientation direction rotated in a plane parallel to the printed circuit board by an orientation angle.

16. (Previously Presented) The memory module of Claim 15, wherein the orientation angle is approximately 180 degrees.

17. (Previously Presented) The memory module of Claim 12, wherein the identical integrated circuits located in the first row of the second lateral portion of the at least one surface of the printed circuit board have a first orientation direction and the identical integrated circuits located in the second row of the second lateral portion of the at least one surface of the printed circuit board have a second orientation direction rotated in a plane parallel to the printed circuit board by an orientation angle.

18. (Previously Presented) The memory module of Claim 17, wherein the orientation angle is approximately 180 degrees.

19. (New) A memory module comprising:

a printed circuit board having a first lateral portion and a second lateral portion;

a plurality of identical integrated circuits mounted on the printed circuit board in a first row and a second row;

a control logic bus connected to the plurality of identical integrated circuits;

a first register connected to the control logic bus, the first register addressing the identical integrated circuits located in the first row and the second row on the first lateral portion and not addressing the identical integrated circuits located in the first row and the second row on the second lateral portion; and

a second register connected to the control logic bus, the second register addressing the identical integrated circuits located in the first row and the second row on the second lateral portion and not addressing the identical integrated circuits located in the first row and the second row on the first lateral portion.